REMARKS/ARGUMENTS

Claims 1-16, 18-20, 23-37, and 55-58 are pending in this application. By this Amendment, Applicant AMENDS Claim 1 and CANCELS Claims 22 and 59.

Support for the amendment to Claim 1 can be found in **Fig. 11** of the present Specification, paragraph no. [0072] of the present Specification, and canceled original Claim 22.

Applicant greatly appreciates the allowance of Claims 2, 3, 5, 7, 9, 11, 13, 18-20, 23, 26, 27, 30, 31, 35-37, 57, and 58 by the Examiner.

The Examiner rejected Claim 59 under 35 U.S.C. § 112, first paragraph as allegedly containing subject matter that was not described in the Specification in such a way as to reasonably convey to one skill in the relevant art that the inventors, at the time of the application was filed, had possession of the claimed invention. Although Applicant respectfully disagrees, in order to expedite prosecution, Applicant has canceled Claim 59. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 59 under 35 U.S.C. § 112, first paragraph.

The Examiner rejected Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55, and 56 under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi (U.S. 2002/0102823) in view of Murakami et al. (U.S. 2002/0068388). The Examiner rejected Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55, and 56 under 35 U.S.C. §103(a) as being unpatentable over Inoue et al. (U.S. 5,693,959) in view of Murakami et al. The Examiner rejected Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55, and 56 under 35 U.S.C. §103(a) as being unpatentable over Takahashi et al. (U.S. 2003/0080384) in view of Murakami et al. The Examiner rejected claims 24, 25, and 32 under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al. in view of Murakami et al., and further in view of Yamazaki et al. (U.S. 2002/0100937).

Applicant respectfully traverses the rejections of Claims 1, 4, 6, 8, 10, 14-16, 22, 24, 25, 28, 29, 32, 55, and 56.

Applicant has amended Claim 1 to recite:

> A semiconductor device, comprising:
> a thin film transistor including a semiconductor layer that includes a

channel region, a source region, and a drain region;

a gate insulating film provided on the semiconductor layer; and

a gate electrode for controlling a conductivity of the channel region; wherein

the gate electrode includes an inclined side surface and a bottom surface which is in contact with a surface of the gate insulating film;

the semiconductor layer is a crystalline semiconductor layer formed through a melting/solidification process;

a surface of the semiconductor layer includes a protruding portion located under the inclined side surface of the gate electrode, **the protruding portion being formed through the melting/solidification process**;

the surface of the gate insulating film has an uneven surface corresponding to the protruding portion formed on the surface of the semiconductor layer;

a cross-section of the gate electrode includes first and second opposing sides that are parallel to each other and a third side that is not parallel to any other side of the cross-section of the gate electrode;

a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer; and

the side surface inclination angle of the gate electrode is an angle between a bottom portion of the inclined side surface of the gate electrode, which is in contact with the surface of the gate insulating film, and the bottom surface of the gate electrode.
(emphasis added)

In the first full paragraph on page 4, the last paragraph on page 6, and the first full paragraph on page 9 of the outstanding Office Action, the Examiner admitted that Yamaguchi, Inoue et al., and Takahashi et al., respectively, fail to teach or suggest a gate electrode having the cross-section as required by Applicant's Claim 1.

The Examiner relied upon Murakami et al. to allegedly cure this deficiency in each of Yamaguchi, Inoue et al., and Takahashi et al. In the paragraph bridging pages 4 and 5, the last full paragraph on page 7, and the paragraph bridging pages 9 and 10 of the outstanding Office Action, the Examiner alleged that it would have been obvious to use the doping implantation process of Marukami et al. in each of the processes of Yamaguchi et al., Inoue et al., and Takahashi et al. for the purpose of modifying the devices of Yamaguchi et al., Inoue et al., and Takahashi et al. by providing regions with different doping concentrations to form Lightly Doped Drain (LDD) regions that are

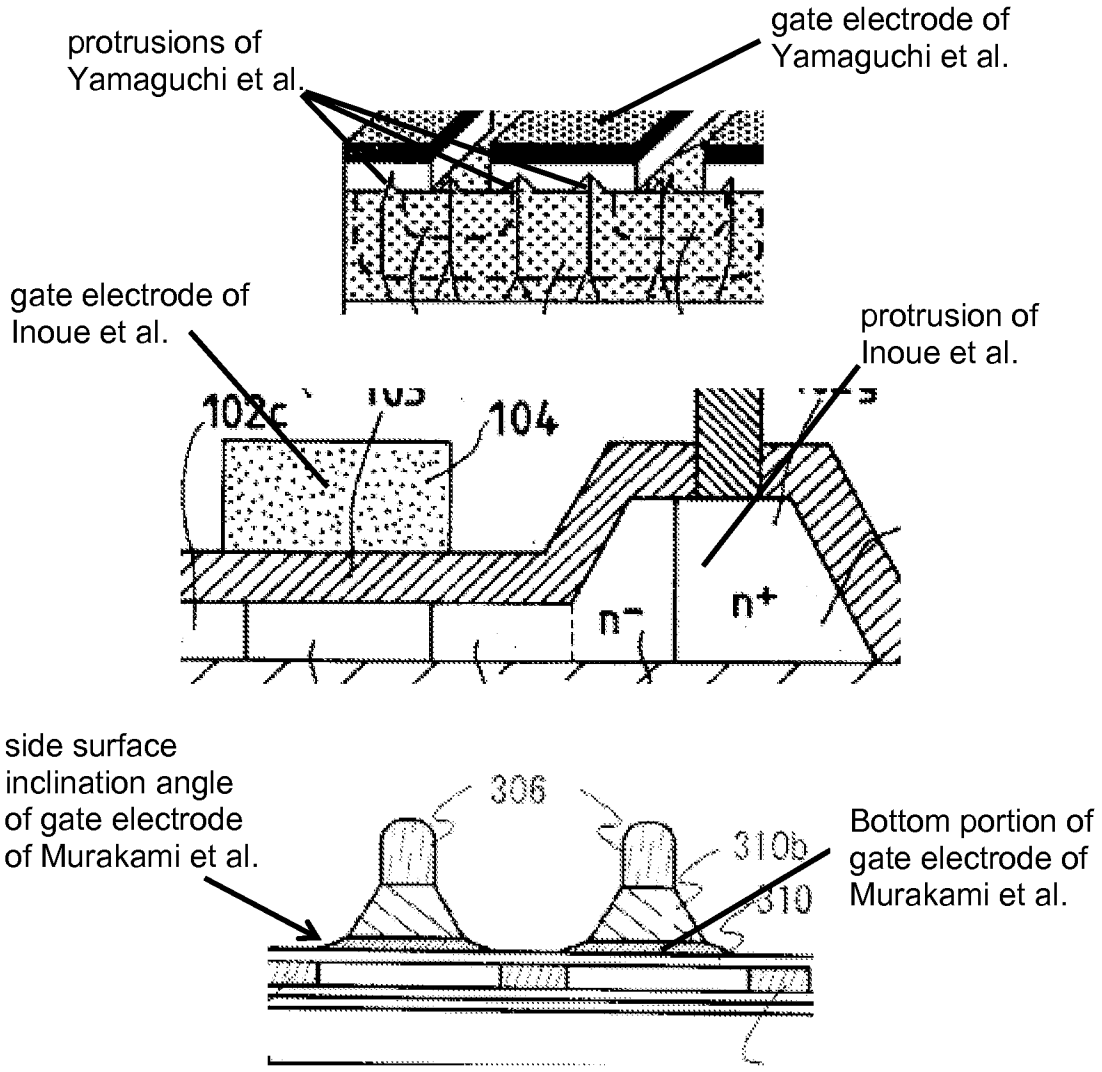
effective in reducing the OFF current value.

Applicant has amended Claim 1 to recite the features of "the semiconductor layer is a crystalline semiconductor layer formed through a melting/solidification process," "the protruding portion being formed through the melting/solidification process," and "a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer," where "the side surface inclination angle of the gate electrode is an angle between a bottom portion of the inclined side surface of the gate electrode, which is in contact with the surface of the gate insulating film, and the bottom surface of the gate electrode." Applicant respectfully submits that the prior art relied upon by the Examiner fails to teach or suggest each of the features recited in Applicant's Claim 1.

With respect to the prior art rejections relying upon the combination of Yamaguchi et al. with Murakami et al. and the combination of Inoue et al. with Murakami et al., Applicant respectfully submits that these combinations fail to teach or suggest the feature of "a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer," where "the side surface inclination angle of the gate electrode is an angle between a bottom portion of the inclined side surface of the gate electrode, which is in contact with the surface of the gate insulating film, and the bottom surface of the gate electrode," as recited in Applicant's Claim 1.

The Examiner has already admitted that neither Yamaguchi et al. nor Inoue et al. teach or suggest the above-quoted feature.

As shown in the following partial, marked-up **Fig. 4** of Yamaguchi, **Fig. 1** of Inoue et al., **Fig. 4b** of Murakami et al. provided below, even if the gate electrodes of Yamaguchi et al. and Inoue et al. are replaced by the gate electrode of Murakami et al., the combinations fail to teach or suggest the above-quoted feature.



The side surface inclination angle of Murakami et al. must be kept small in order to allow the LDD region to be formed. If the side surface inclination angle of Murakami et al. is large, then no LDD region or a very small LDD region will be formed, which will not effectively reduce the OFF current value of the modified device of Yamaguchi et al. and Inoue et al.

Thus, neither the combination of Yamaguchi et al. with Murakami et al. nor the combination of Inoue et al. with Murakami et al. teaches or suggests the feature of “a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer,” where “the side surface inclination

angle of the gate electrode is an angle between a bottom portion of the inclined side surface of the gate electrode, which is in contact with the surface of the gate insulating film, and the bottom surface of the gate electrode," as recited in Applicant's Claim 1.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 1 under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi in view of Murakami et al. and the rejection of Claim 1 under 35 U.S.C. §103(a) as being unpatentable over Inoue et al. in view of Murakami et al.

With respect to the prior art rejection relying upon the combination of Takahashi et al. with Murakami et al., Applicant respectfully submits that this combination fails to teach or suggest the features of "the semiconductor layer is a crystalline semiconductor layer formed through a melting/solidification process" and "the protruding portion being formed through the melting/solidification process" as recited in Applicant's Claim 1.

In the paragraph bridging pages 8 and 9 of the outstanding Office Action, the Examiner alleged that semiconductor layer **71** of Takahashi et al. includes protruding portions.

As explained in paragraph nos. [0004] and [0017] of Takahashi et al., the protruding portions of Takahashi et al. are formed by a step-controlled epitaxial growth technique. That is, Takahashi et al. fails to teach or suggest that the protruding portions of Takahashi et al. are formed by a melting/solidification process as recited in Applicant's Claim 1. The Examiner implicitly admits this failure of Takahashi et al. by failing to explicitly address this feature that was original recited in now canceled Claim 22 in the body of the rejection on pages 8-10 of the outstanding Office Action.

Further, the Examiner is respectfully reminded that the patentability of the structure implied by product-by-process limitations must be considered. MPEP § 2113 states

> >The structure implied by the process steps [in product-by-process claims] should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., In re Garnero, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979) (holding "interbonded by

interfusion" to limit structure of the claimed composite and noting that terms such as "welded," "intermixed," "ground in place," "press fitted," and "etched" are capable of construction as structural limitations.)<.

Applicants respectfully submit that the prior art of record fails to provide any evidence that a structure of the protruding portions of Takahashi et al. that are formed a step-controlled epitaxial growth technique share any similarities with the structure of the protruding portions recited in Applicant's Claim 1 that are formed by a melting/solidification process.

Murakami et al. fails to teach or suggest that any protrusions are formed and certainly fails to teach or suggest the feature of "the protruding portion being formed through the melting/solidification process" as recited in Applicant's Claim 1.

Thus, Applicant respectfully submits that the combination of Takahashi et al. and Murakami et al. fails to teach or suggest the features of "the semiconductor layer is a crystalline semiconductor layer formed through a melting/solidification process" and "the protruding portion being formed through the melting/solidification process" as recited in Applicant's Claim 1.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 1 under 35 U.S.C. §103(a) as being unpatentable over Takahashi et al. in view of Murakami et al.

The Examiner has relied upon Yamazaki et al. to allegedly cure various deficiencies in the combination of Yamaguchi et al. and Murakami et al. However, Yamazaki et al., Yamaguchi et al., and Murakami et al., applied alone or in combination with, fail to teach or suggest the feature of "a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer," where "the side surface inclination angle of the gate electrode is an angle between a bottom portion of the inclined side surface of the gate electrode, which is in contact with the surface of the gate insulating film, and the bottom surface of the gate electrode," in combination with the other features recited in Applicant's Claim 1.

Accordingly, Applicant respectfully submits that the prior art of record, applied alone or in combination, fails to teach or suggest the unique combination and

arrangement of elements recited in Claim 1 of the present application. Claims 4, 6, 8, 10, 14-16, 22, 24, 25, 28, 29, 32, 55, and 56 depend upon Claim 1 and are therefore allowable for at least the reasons that Claim 1 is allowable.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicant petitions the Commissioner for a ONE-month extension of time, extending to April 4, 2007, the period for response to the Office Action dated December 4, 2006.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Dated: April 4, 2007

/Peter Medley #56,125/
Attorneys for Applicant

KEATING & BENNETT, LLP
8180 Greensboro Drive, Suite 850
Tyson's Corner, VA 22102
Telephone: (703) 637-1480
Facsimile: (703) 637-1499

Joseph R. Keating
Registration No. 37,368

Peter Medley
Registration No. 56,125